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DOCKET NO.: S1022.80854US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jacques PRUNIER
Serial No.: 10/083,714 Patent No. 6,938,194 *B2*
Filed: February 26, 2002 Issued: August 30, 2005
For: INTEGRATED CIRCUIT TESTING METHOD AND SYSTEM

Examiner: John P. Trimmings
Art Unit: 2133 Confirmation No.: 3976

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate
SEP 15 2005
of Correction

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

- ☒ Request for Certificate of Correction
- ☒ Pages 1-3, 5-8 and 10 Apl as Filed and Cols 1 and 3-8 of U.S. Patent No. 6,938,194
- ☒ PTO Form SB/44
- ☒ Return Postcard

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617)646.8000, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Correspondence and Mail Division, Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on September 6, 2005.

Attorney Docket No.: S1022.80854US00
XNDD

Respectfully submitted,

Jacques Prunier, Applicant

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**REQUEST FOR CERTIFICATE
OF CORRECTION UNDER 37 C.F.R. §1.322**

Sir/Madam:

Patentee respectfully request the correction of errors found in the above-captioned patent. Specifically, there are typographical errors throughout the specification of issued U.S. 6,938,194.

Patentee submits below a reproduction of the sentence as it appears in the application as filed followed by the corresponding text as it appears in the issued patent. The text where an error has been found will be identified in bold lettering.

1) Page 1, lines 25-26 of the application as filed read as shown below:

Mi is connected to the input Di of same **rank**. A **first** input terminal of each multiplexer Mi is connected to output terminal Oi of block LB. (Emphasis added)

Column 1, lines 46-48 of U.S. Patent No. 6,938,194 read as shown below:

Mi is connected to the input Di of same **r**. A **fast** input terminal of each multiplexer Mi is connected to output terminal Oi of block LB. (Emphasis added)

The word "rank" has erroneously been changed to --r-- and the word "first" has erroneously been changed to --fast-- in the issued patent.

2) Page 2, line 9 of the f the application as filed reads as shown below:

test register. Test data TD3, TD2, and TD1 are successively presented to **terminal** SI at the rate of (Emphasis added)

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Column 1, line 65-67 of U.S. Patent no. 6,938,194 reads as shown below:

test register. Test data TD3, TD2, and TD1 are successively presented to SI at the rate of

The word "terminal" has been omitted from the issued patent.

3) Page 3, line 20 of the application as filed reads as shown below:

inactive and multiplexer 6 transmits signal RS without influencing the circuit **operation**. When the (Emphasis added)

Column 2, line 66 through column 3, line 2 of U.S. Patent no. 6,938,194 read as shown below:

inactive and multiplexer 6 transmits signal RS without influencing the circuit **operator**. When the (Emphasis added)

The word "operation" has erroneously been amended to read --operator--.

4) Page 5, line 17 of the application as filed reads as shown below:

reactivating the register connection of the flip-flops before sequentially **reading** the data contained in (Emphasis added)

Column 4, lines 21-22 of U.S. Patent no. 6,938,194 reads as shown below:

reactivating the register connection of the flip-flops before sequentially **wading** the data contained in (Emphasis added)

The word "reading" has erroneously been amended to read --wading--.

5) Page 6, line 8 of the application as filed reads as shown below:

inhibiting means 4, 6, and 10, identical to the elements **bearing** the same references in Fig. 3, (Emphasis added)

Column 4, lines 54-55 of U.S. Patent no. 6,938,194 reads as shown below:

inhibiting means 4, 6, and 10, identical to the elements **beating** the same references in Fig. 3, (Emphasis added)

The word "bearing" has erroneously been amended to read --beating--.

6) Page 7, line 23 of the application as filed reads as shown below:

not include an error **that** maintains signal EN1 active. (Emphasis added)

Column 5, line 55 of U.S. Patent no. 6,938,194 reads as shown below:

not include an error **at** maintains signal EN1 active. (Emphasis added)

The word "that" has erroneously been amended to read --at--.

7) Page 8, line 15 of the application as filed reads as shown below:

vector TD6, TD5, and TD4 is input into the **test** register. Vector TD6, TD5, and TD4 is chosen to (Emphasis added)

Column 6, lines 22-23 of U.S. Patent no. 6,938,194 reads as shown below:

vector TD6, TD5, and TD4 is input into the **lest** register. Vector TD6, TD5, and TD4 is chosen to (Emphasis added)

The word "test" has erroneously been amended to read --lest--.

8) Page 8, line 27 of the application as filed reads as shown below:

respectively stored in flip-flops FF3, FF2, and FF1 and provided to input **terminals** I3, I2, and I1 from (Emphasis added)

Column 6, lines 41-42 of U.S. Patent no. 6,938,194 reads as shown below:

respectively stored in flip-flops FF3, FF2, and FF1 and provided to input I3, I2, and I1 from

The word "terminals" has been omitted.

9) Page 10, line 9 of the application as filed reads as shown below:

improvements which will **readily** occur to those skilled in the art. Disturbing elements 2, 5, and 8 (Emphasis added)

Column 7, lines 40-42 of U.S. Patent no. 6,938,194 reads as shown below:

improvements which will **really** occur to those skilled in the art. Disturbing elements 2, 5, and 8 (Emphasis added)

The word "readily" has erroneously been amended to read --really--.

10) Page 10, line 10 of the application as filed reads as shown below:

shown in Fig. 4 are shown as an example only. There are many **types** of elements disturbing the scan (Emphasis added)

Column 7, lines 42-43 of U.S. Patent no. 6,938,194 reads as shown below:

shown in Fig. 4 are shown as an example only. There are many **steps** of elements disturbing the scan (Emphasis added)

The word "types" has erroneously been amended to read --steps--.

11) Page 10, line 27 of the application as filed reads as shown below:

block and three **flip-flops**, but those skilled in the art will easily adapt the present invention to a circuit (Emphasis added)

Column 8, lines 2-4 of U.S. Patent no. 6,938,194 reads as shown below:

block and three **flip:ops**, but those skilled in the art will easily adapt the present invention to a circuit (Emphasis added)

The word "flip-flops" has erroneously been amended to read --flip:ops--.

Support for the requested corrections can be found in enclosed, highlighted copy of pages 1-3, 5-8 and 10 of the application as filed and columns 1 and 3-8 of U.S. Patent No. 6,938,194. Also enclosed is PTO form SB/44.

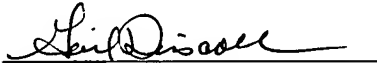
The corrections requested do not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the correction be made and that a Certificate of Correction be issued.

None of the above amendments were made by either Patentee or the Examiner. Therefore, Patentee respectfully submits that, since the errors for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

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INTEGRATED CIRCUIT TESTING METHOD AND SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an improved method and system for functionally testing an integrated circuit.

2. Discussion of the Related Art

In a functional testing, it is checked whether an integrated circuit performs the functions for which it has been designed. Predetermined signals are provided to the inputs of the circuit or of determined circuit blocks and the outputs are read to determine whether they correspond to an expected answer. To test all the possible errors of an integrated circuit, a first approach consists of providing the integrated circuit with all the possible combinations of input states and of checking all the signals provided as a response by the circuit. This, however, can take a long time. Error models enable determining the test signals (or test vectors) most adapted to testing a circuit.

A so-called scan test method, applied to a logic block of an integrated circuit, having each of its inputs connected to an output terminal of a flip-flop and each of its outputs connected to an input terminal of a flip-flop, will more specifically be considered herein. A scan test system includes means for controlling the writing and the reading of test signals in said flip-flops.

FIG. 1 schematically shows a scan test system associated with an integrated circuit including a combinatorial logic block, or logic block LB. The circuit includes three flip-flops FF1, FF2, and FF3. Input and output terminals D1 and Q1 of flip-flop FF1 are respectively coupled to an output terminal O1 and to an input terminal I1 of block LB. Similarly, the input and output terminals D2, Q2, and D3, Q3 of flip-flops FF2 and FF3 are respectively coupled to output and input terminals O2, I2, and O3, I3 of block LB. Clock terminals CK1, CK2, and CK3 of flip-flops FF1, FF2, and FF3 receive a same clock signal CLK. Flip-flops FF1, FF2, and FF3, as well as logic block LB, form the functional part of the circuit. The circuit test system includes multiplexers Mi (where i ranges between 1 and 3), each associated with the flip-flop FFi of the same rank. The output terminal of each multiplexer Mi is connected to the input Di of same i. A fast input terminal of each multiplexer Mi is connected to output terminal Oi of block LB. A control terminal of each multiplexer Mi receives a signal SC. The second input terminal of multiplexer M1 is connected to an input terminal SI of the circuit. The second input terminals of multiplexers M2 and M3 are respectively connected to output terminals Q1 and Q2 of flip-flops FF1 and FF2. Terminal Q3 of flip-flop FF3 is connected to an output terminal SO of the circuit.

Outside of test periods, signal SC is inactive and multiplexers Mi are controlled so that outputs Oi of the logic block are connected to inputs Di of flip-flops FFi. When signal SC is active, multiplexers Mi are controlled so that flip-flops FFi form a FIFO-type test register rated by clock signal CLK.

FIG. 2 schematically illustrates the operation of the test system of FIG. 1.

In a first step, signal SC is maintained active so that flip-flops FF1, FF2, and FF3 form the test register. Test data TD3, TD2, and TD1 are successively presented to SI at the rate of pulses of clock signal CLK, at times t1, t2, and t3. At

time t3, data TD3, TD2, and TD1 are respectively stored in flip-flops FF3, FF2, and FF1. Data TD3', TD2', and TD1' are then presented on output terminals O3, O2, and O1 of logic block LB.

In a second step, after time t3, signal SC is made inactive so that the multiplexers connect output terminals O3, O2, and O1 of the logic block to input terminals D3, D2, and D1 of the flip-flops. At the next pulse of signal CLK, at a time t4, data TD3', TD2', and TD1' are stored in flip-flops D3, D2, and D1. Signal SC is made active again after time t4.

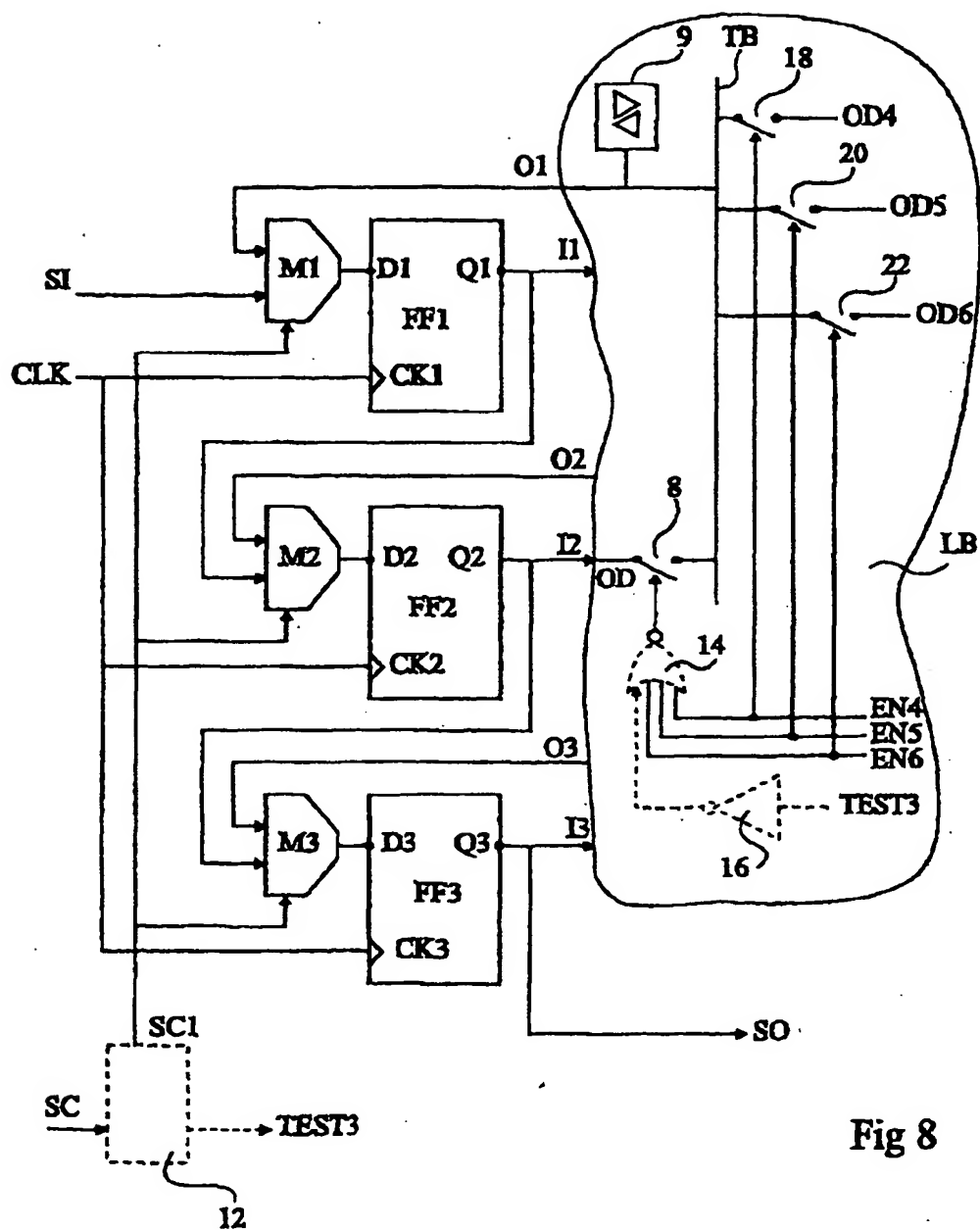
In a third step, starting from the reactivation of signal SC, data TD3', TD2', and TD1' are shifted in the test register at the rate of pulses of clock signal CLK, at times t5 and t6, and are successively provided to terminal SO. During this shift, a new test vector TD6, TD5, TD4 is input in the register. Data TD3', TD2', and TD1' provided to terminal SO are compared with their expected values, generally logic "0s" or "1s".

These three steps are repeated many times as test vectors have been provided. The analysis of the data provided by the logic block as a response to the test data, collected during each third step, enables determining whether the circuit includes defective elements. A defective element is, according to the error model conventionally used, an element having an output abnormally fixed to 0 or to 1. Such a test system operates satisfactorily if the logic block includes no element capable of disturbing the operation of the test register, or to disturb the propagation of the signals in the logic block. Even if such disturbing elements exist, existing test systems are adapted to inhibiting them.

FIG. 3 schematically shows a test system for an integrated circuit similar to the circuit shown in FIG. 1, in which three types of disturbing elements have been inserted.

A first disturbing element is an AND gate 2, a first input of which receives clock signal CLK, the second input of which is coupled to a clock enable signal EN1 generated in block LB, and the output of which is connected to terminal CK2. Gate 2 is capable of disturbing the sequencing of the test register, if for example data provided to block LB cause the inactivation of signal EN1 and the blocking of flip-flop FF2. The flip-flop assembly can then no longer operate as a shift register during the test. To solve this type of problem and make the circuit testable, a solution provided in prior art consists of adding an OR gate 4, the output final of which is connected to the second input terminal of AND gate 2, a first input terminal of which receives clock enable signal EN1, and a second input terminal of which receives a control signal TEST. When the circuit is not tested, signal TEST is made inactive, gate 4 transmits signal EN1 to gate 2 without influencing the circuit operation. When the circuit is tested, signal TEST is activated, the output of gate 4 remains activated whatever signal EN1, and gate 2 is no longer capable of disturbing the sequencing of the test register.

A second disturbing element is an element 5 which provides a reset signal RS to a reset terminal RST of flip-flop FF3 via an output terminal O5. Element 5 is capable of disturbing the sequencing of the test register, if for example test data provided to block LB cause the activation of signal RS and the resetting of flip-flop FF3. To make the circuit testable, a multiplexer 6 having an output terminal connected to terminal RST of flip-flop FF3 and a first input terminal connected to output O5 of the logic block has been added. A second input of multiplexer 6 receives a controllable signal TRST, for example permanently inactive. When the circuit is not tested, signal TEST is made inactive and multiplexer 6 transmits signal RS without influencing the



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circuit operator. When the circuit is tested, signal TEST is made active and multiplexer 6 permanently provides controllable signal TRST to terminal RST of flip-flop FF3. Thereby, block 5 is not capable of disturbing the sequencing of the test register.

A third disturbing element is a switch 8 capable of disturbing the propagation of a signal OD provided by block LB to output terminal O1. Terminal O1 is connected to a signal storage element 9 and switch 8 receives a signal EN2 generated by block LB. Switch 8 is capable of disturbing the circuit testing, especially during a second step of the testing, if test data provided to block LB cause the inactivation of signal EN2 and the opening of switch 8. Storage element 9 then provides the last value of the signal that it has received. The logic circuit is no longer combinatorial and it is no longer testable by scanning. To make the circuit testable, an OR gate 10, an output of which is connected to control switch 8, a first input terminal of which receives enable signal EN2, and a second input terminal of which receives signal TEST has been added. When the circuit is not tested, signal TEST is made inactive and gate 10 transmits signal EN2 to switch 8 without influencing the circuit operation. When the circuit is tested, signal TEST is made active, the output of gate 10 remains activated whatever signal EN2, and switch 8 remains closed and is no longer capable of disturbing the circuit testing.

When signal TEST is made active, the operation of the test system shown in FIG. 3 is similar to the operation illustrated in FIG. 2 of the test system of FIG. 1.

A disadvantage of the test system of FIG. 3 is that it does not enable testing the proper operation of elements 2, 5, and 8 inhibited by inhibiting means 4, 6, and 10 of the test system. The testing of elements 2, 5, and 8 must then be performed by means of specific test vectors, without using the test system. As the size and complexity of integrated circuits increases, the number of disturbing elements becomes significant and it becomes difficult to provide all the necessary specific test vectors.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a test system and method enabling testing of as many elements of an integrated circuit as possible.

For this purpose, the present invention provides a scan test system provided with means for testing the elements disturbing the test.

To achieve this and other objects, the present invention provides a system for testing an integrated circuit, the integrated circuit including flip-flops connected to a logic block and the test system including means for connecting the flip-flops as a register, means for inhibiting the different elements of the logic block capable of disturbing the sequencing of the register or the propagation of the signals into the logic block and a control means for separately controlling the different means of inhibition of said elements of the logic block and the means for connecting the flip-flops as a register.

According to an embodiment of the present invention, said elements of the logic block are of several types, and the control means is provided to control together the means of inhibition of the elements of a same type.

According to an embodiment of the present invention, elements of a first type condition the clock signal provided to at least one flip-flop.

According to an embodiment of the present invention, elements of a second type condition a reset signal provided to at least one flip-flop.

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According to an embodiment of the present invention, elements of a third type include locking elements capable of preventing the propagation of at least one signal into the logic block.

The present invention also aims at a method for testing an integrated circuit including flip-flops connected to a logic block, especially including the steps of:

a) connecting the flip-flops as a register and inhibiting the elements of the logic block capable of disturbing the register sequencing, these elements being gathered in sets of elements of same type, then writing a test vector into the register,

b) reactivating a set of elements, then clocking the flip-flops, and

c) inhibiting again the set of reactivated elements before sequentially reading the data contained in the register.

According to an embodiment of the present invention, step b) also includes deactivating the register connection of the flip-flops before clocking the flip-flops, and step c) also includes reactivating the register connection of the flip-flops before sequentially reading the data contained in the register.

The foregoing objects, features and advantages of the present invention, will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1, previously described, schematically shows a conventional system for testing by scanning an integrated circuit;

FIG. 2, previously described, illustrates the operation of the test system of FIG. 1;

FIG. 3, previously described, schematically shows a conventional integrated circuit scan test system including elements disturbing the test system;

FIG. 4 schematically shows an embodiment of a test system according to the present invention;

FIG. 5 illustrates the testing of a first disturbing element of the circuit of FIG. 4;

FIG. 6 illustrates the testing of a second disturbing element of the circuit of FIG. 4;

FIG. 7 illustrates the testing of a third disturbing element of the circuit of FIG. 4; and

FIG. 8 schematically shows an embodiment of a test system according to the present invention.

DETAILED DESCRIPTION

FIG. 4 schematically shows a scan test system according to the present invention, associated with an integrated circuit such as shown in FIG. 3. The test system includes multiplexers Mi and inhibiting means 4, 6, and 10, identical to the elements bearing the same references in FIG. 3, connected in a similar way except for their control terminals. According to the present invention, each type of inhibiting means is controlled by a specific control signal. Inhibiting means 4, 6 and 10 respectively receive a control signal TEST1, TEST2, and TEST3 provided by a control means 12. Also according to the present invention, multiplexers Mi are controlled by a control signal SC1 provided by control means 12, which receives control signal SC. Control means 12 is provided to generate signals TEST1, TEST2, TEST3, and SC1 based on signal SC.

When idle, the test system according to the present invention has no influence upon the circuit operation.

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According to a first operating mode, a control means 12 provides multiplexers Mi with a signal SC1 identical to signal SC and it maintains control signals TEST1, TEST2, and TEST3 active. Thus, inhibiting means 4, 6, and 10 are activated and the effect of the disturbing elements is inhibited. The operation of the test system is then similar to the operation of the test system of FIG. 3. This first operating mode enables performing a conventional scan test of the circuit. During this first operating mode, disturbing elements 2, 5, and 8 are not tested.

According to a second operating mode, illustrated by FIGS. 5, 6, and 7, control means 12 successively controls the testing of each disturbing element, especially by temporarily inhibiting the effects of the tested disturbing element, and by permanently inhibiting the effects of the other untested disturbing elements. For reasons of writing simplicity, references TD1 to TD6 and t1 to t6 already used in FIG. 2, but which represent different test data and times in the different drawings, are used in the following FIGS. 5, 6, and 7.

FIG. 5 illustrates the testing of disturbing element 2. During the entire testing duration, control signals TEST2, TEST3, and SC1 are maintained active, so that flip-flops FF1, FF2, and FF3 form the test register and that the effect of disturbing elements 5 and 8 is inhibited. Control signal TEST1 is equal to signal SC received by block 12.

In a first step, signal TEST1 is maintained active so that signal EN1 provided by block LB to element 2 is not capable of disturbing the sequencing of the test register. Test data TD3, TD2, and TD1 are successively presented to terminal SI at the rate of the pulses of clock signal CLK, at times t1, t2, and t3, so that data TD3, TD2, and TD1 are respectively stored in flip-flops FF3, FF2, and FF1 from time t3. The test vector corresponding to data TD3, TD2, and TD1 is chosen to give to logic block LB a state such that signal EN1 is normally active.

In a second step, a predetermined duration after time t3, signal TEST1 is made inactive so that gate 4 transmits signal EN1 to element 2. If element 2 or its connection exhibits an error and signal EN1 is inactive, instead of being active as it should be, flip-flop FF2 is not clocked at the next pulse of signal CLK, at a time t4. Datum TD2 then remains stored in flip-flop FF2 after time t4, while datum TD1 should have been input into flip-flop FF2.

In a third step, control signal TEST1 is made active again, a predetermined duration after time t4. The data contained in flip-flops FF1, FF2, and FF3 are shifted in the test register at the rate of the pulses of clock signal CLK, at times t5 and t6, and successively provided to terminal SO to be analyzed.

At times t4, t5, and t6, a new test vector TD6, TD5, and TD4 is input into the test register. This new test vector is chosen to give the logic block a state in which signal EN1 is normally inactive. The preceding second and third steps are then repeated to check that element 2 or its connection do not include an error at maintains signal EN1 active.

FIG. 6 illustrates the testing of disturbing element 5. Control signals TEST1, TEST3, and SC1 are maintained active, so that flip-flops FF1, FF2, and FF3 form the test register and the effect of disturbing elements 2 and 8 is inhibited. Control signal TEST2 is equal to signal SC received by block 12.

In a first step, signal TEST2 is maintained active so that signal RS provided by element 5 is not capable of disturbing the sequencing of the test register. Test data TD3, TD2, and TD1 are successively presented to terminal SI at the rate of pulses of clock signal CLK, at times t1, t2, and t3, so that data TD3, TD2, and TD1 are respectively stored in flip-flops

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FF3, FF2, and FF1 and provided to input terminals I3, I2, and I1 from time t3. Data TD3, TD2, and TD1 form a test vector intended for controlling the activation of signal RS by element 5. Thus, in a normal operation of the logic block, signal RS would cause a reset of the content of flip-flop FF3. During the first step, nothing occurs due to the presence of signal TEST2 in an active state.

In a second step, at a time t3' subsequent to time t3, control signal TEST2 is made inactive so that signal RS directly controls the reset terminal of flip-flop FF3. If element 5 or its connection includes an error that maintains signal RS inactive, flip-flop FF3 is not reset and datum TD3 remains stored in flip-flop FF3 during the period shown with hatchings in FIG. 6. Further, at the next pulse of signal CLK, which occurs at a time t4, datum TD2 is stored in flip-flop FF3 instead of flip-flop FF3 to remain reset. If signal RS is active, datum TD3 is replaced in flip-flop FF3 by a reset value and flip-flop FF3 remains reset after time t4.

In a third step, control signal TEST2 is made active again, a predetermined duration after time t4. At time t4 and at times t5 and t6 representing the next pulses of clock signal CLK, a new test vector TD6, TD5, and TD4 is input into the test register. Vector TD6, TD5, and TD4 is chosen to give the logic block a state in which signal RS is deactivated by element 5. The preceding second step is then repeated to check that element 5 or its connection does not include an error that maintains signal RS active.

FIG. 7 illustrates the testing of disturbing element 8. Control signals TEST1 and TEST2 are maintained active so that the effect of disturbing elements 2 and 8 is not inhibited. Control signals TEST3 and SC1 are equal to signal SC received by block 12.

In a first step, control signal SC1 is made active so that flip-flops FF1, FF2, and FF3 form the test register. Control signal TEST3 is also active, and the propagation of signal OD provided by block LB to terminal O1 is not capable of being disturbed by switch 8, whatever the value of signal EN2 provided to switch 8. Test data TD3, TD2, and TD1 are successively presented to terminal SI at the rate of pulses of clock signal CLK, at times t1, t2, and t3, so that data TD3, TD2, and TD1 are respectively stored in flip-flops FF3, FF2, and FF1 and provided to input I3, I2, and I1 from time t3. The data which are then presented on outputs O3, O2, and O1 of block LB are called TD3', TD2', and TD1'. Storage element 9 stores value TD1'.

In a second step, a predetermined duration after time t3, control signals TEST3 and SC1 are made inactive. Signal EN2 then directly controls switch 8 and the multiplexers connect output terminals O3, O2, and O1 of the logic block to input terminals D3, D2, and D1 of the flip-flops. At the next pulse of signal CLK, at a time t4, data TD3', TD2', and TD1' are stored in flip-flops D3, D2, and D1. Data TD3', TD2', and TD1' are then provided by the flip-flops to terminals I3, I2, and I1 of the logic block. The value taken by OD after time t4 is called TD1". Data TD3', TD2', and TD1" form a test vector chosen to give block LB a state in which signal EN2 is inactive and controls the opening of switch 8. If switch 8 or its connection have an error that maintains switch 8 closed, datum TD1" is provided to flip-flop FF1 after time t4, as illustrated. If switch 8 has no error and signal EN2 controls the opening of switch 8 at time t4, datum TD1" is not provided to flip-flop FF1, and flip-flop FF1 keeps datum TD1'.

In a third step, signals SC1 and TEST3 are made active again a predetermined duration after time t4. The data contained in flip-flops FF1, FF2, and FF3 are shifted in the

test register at the rate of the pulses of clock signal CLK, at times t5 and t6, and successively provided to terminal SO.

At times t4, t5, and t6, a new test vector TD6, TD5, and TD4, for example chosen to give block LB a state in which signal EN2 is active, is input into the test register. The preceding second and third steps are then repeated to check that switch 8 is not maintained closed.

A test system according to the present invention thus enables testing the elements disturbing the scan test, which is a first advantage.

Block 12 generates signals TEST1, TEST2, TEST3, and SC1 based on signal SC. Thus, a test system according to the present invention enables testing the elements disturbing the scan test without using a large number of specific test terminals intended for each receiving one of signals TEST1, TEST2, TEST3, and SC1, which is an additional advantage of the present invention.

The shown circuit includes, as an example, a single disturbing element of each type. When a circuit includes several disturbing elements of same type, that is, each having a same effect on similar elements of the circuit, the present invention provides controlling the means for inhibiting these disturbing elements of same type with a same control signal provided by means 12. Such a control of the inhibiting means especially enables rapidly testing the disturbing elements by means of a small number of test vectors, which is an additional advantage of the present invention.

The control means, of simple structure, has a reduced size. Thus, a test system according to the present invention has substantially the same size as a conventional scan test system, which is an additional advantage of the present invention.

Further, since the present invention provides isolating the testing of each type of disturbing element, the test vectors used for each type of disturbing element can be generated automatically and rapidly by a calculator having a list of the circuit elements and of their connections. This is an additional advantage of the present invention.

Of course, the present invention is likely to have various alterations, modifications, and improvements which will really occur to those skilled in the art. Disturbing elements 2, 5, and 8 shown in FIG. 4 are shown as an example only. There are many steps of elements disturbing the scan test, generally known as "exceptions to the rules of scan testability", and those skilled in the art will easily adapt the present invention to the types of disturbing elements which have not been shown herein.

FIG. 8 schematically shows an embodiment of a test system according to the present invention, adapted to the testing of a specific disturbing element 8. The preceding disturbing elements 2 and 5 have not been shown in FIG. 8. In FIG. 8, signal OD is directly provided by the output of flip-flop FF2, and terminal O1 and storage element 9 are connected to a three-state bus TB. Bus TB further receives signals OD4, OD5, OD6 via switches 18, 20, and 22. Switches 18, 20, and 22 receive signals EN4, EN5, EN6 from block LB. Switch 8 is controlled by a NOR gate receiving signals EN4, EN5, EN6 and the inverse of signal TEST3 as an input. When signal TEST3 is activated, terminal O1 is controlled either by signals OD4, OD5, OD6, or by flip-flop FF2, and the circuit remains combinatorial whatever the state of signals EN4, EN5, EN6.

The test steps and vectors of disturbing elements 2, 5, and 8 have also been described as an example, but those skilled in the art will easily adapt the present invention to other test steps and to other test vectors.

The present invention has been described in relation with a circuit including a single logic block and three flip-flops, but those skilled in the art will easily adapt the present invention to a circuit including a greater number of logic blocks and/or a greater number of flip-flops. If the circuit includes several logic blocks, each logic block may be tested separately.

Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:

1. A system for testing an integrated circuit, the integrated circuit including flip-flops connected to a logic block and the test system including:

test means operable for connecting the flip-flops as a register, and

a plurality of types of inhibition means, each type of inhibition means being operable for inhibiting one specific type of element of the logic block having a configuration that can disturb the sequencing of the register or the propagation of signals into the logic block, and

control means having:

a first operating mode for operating the test means in synchronism with a command signal while operating continuously the inhibition means; and

a second operating mode for operating inhibition means of a first of the plurality of types of inhibition means in synchronism with the command signal while operating continuously inhibition means of a type different than the first type and the test means, or for operating simultaneously the test means and inhibition means of a first of the plurality of types of inhibition means in synchronism with the command signal while operating continuously inhibition means of a type different than the first type.

2. The integrated circuit test system of claim 1, wherein elements of a first type condition a clock signal provided to at least one flip-flop.

3. The integrated circuit test system of claim 2, wherein said elements of the first type include means for activating or inactivating said clock signal.

4. The integrated circuit test system of claim 1, wherein elements of a second type condition a reset signal provided to at least one flip-flop.

5. The integrated circuit test system of claim 1, wherein elements of a third type include locking elements capable of preventing the propagation of at least one signal into the logic block.

6. Scan test circuitry in an integrated circuit having a logic block including elements capable of disturbing a scan test, comprising:

a plurality of flip-flops operable as a register in a scan test mode;

inhibiting circuits for inhibiting each of the disturbing elements of the logic block from disturbing a scan test; and

a controller for successively controlling each of the inhibiting circuits individually during a scan test.

7. Scan test circuitry as defined in claim 6, wherein the controller is configured to load into the flip-flops, with all disturbing elements inhibited, a test vector for testing a first disturbing element and, subsequently, to enable the first

disturbing element and to observe operation of the logic block in response to the test vector.

8. Scan test circuitry as defined in claim 7, wherein the controller is configured to scan test the first disturbing element in an active state in response to a first test vector and to scan test the first disturbing element in an inactive state in response to a second test vector.

9. Scan test circuitry as defined in claim 6, wherein the controller is configured to individually scan test each of the disturbing elements in active and inactive states.

10. Scan test circuitry as defined in claim 6, wherein the controller is configured to:

load into the flip-flops, with all disturbing elements inhibited, a first test vector for scan testing a first disturbing element in an active state;

enable the first disturbing element with all other disturbing elements inhibited;

observe operation of the logic block in response to the first test vector;

load into the flip-flops, with all disturbing elements inhibited, a second test vector for scan testing the first disturbing element in an inactive state;

enable the first disturbing element with all other disturbing elements inhibited; and

observe operation of the logic block in response to the second test vector.

11. Scan test circuitry as defined in claim 6, wherein the controller is further configured to perform a scan test with all disturbing elements inhibited by the respective inhibiting circuits.

12. Scan test circuitry as defined in claim 6, wherein at least one of the inhibiting circuits is configured to inhibit a disturbing element that affects a clock signal supplied to at least one of the flip-flops.

13. Scan test circuitry as defined in claim 6, wherein at least one of the inhibiting circuits is configured to inhibit a disturbing element that affects a reset signal supplied to at least one of the flip-flops.

14. Scan test circuitry as defined in claim 6, wherein at least one of the inhibiting circuits is configured to inhibit a disturbing element that affects at least one input from the scan test circuitry to the logic block.

15. Scan test circuitry as defined in claim 6, wherein at least one of the inhibiting circuits is configured to inhibit a disturbing element that affects at least one output of the logic block to the scan test circuitry.

16. In an integrated circuit having a plurality of flip-flops operable as a register in a scan test mode and a logic block including elements capable of disturbing a scan test, each of the elements having a type, a scan test method comprising:

(a) inhibiting all of the disturbing elements except a plurality of disturbing elements of a selected type;

(b) performing a scan test of the disturbing elements of the selected type;

(c) repeating steps (a) and (b) for each type of disturbing element in the logic block;

(d) performing a scan test of the logic block with all of the disturbing elements inhibited.

17. A scan test method as defined in claim 16, wherein performing a scan test of the selected disturbing elements comprises loading into the flip-flops a first test vector for scan testing the selected disturbing elements in an active

state and observing operation of the logic block in response to the first test vector.

18. A scan test method as defined in claim 17, wherein performing a scan test of the selected disturbing elements further comprises loading into the flip-flops a second test vector for scan testing the selected disturbing elements in an inactive state and observing operation of the logic block in response to the second test vector.

19. A scan test method as defined in claim 16, wherein inhibiting all of the disturbing elements except disturbing elements of a selected type comprises inhibiting disturbing elements except those of a type that affects a clock signal supplied to at least one of the flip-flops.

20. A scan test method as defined in claim 16, wherein inhibiting all of the disturbing elements except disturbing elements of a selected type comprises inhibiting disturbing elements except those of a type that affects a reset signal supplied to at least one of the flip-flops.

21. A scan test method as defined in claim 16, wherein inhibiting all of the disturbing elements except disturbing elements of a selected type comprises inhibiting disturbing elements except those of a type that affects a locking element coupled to at least one of the flip-flops.

22. A scan test method as defined in claim 16, wherein inhibiting all of the disturbing elements except disturbing elements of a selected type comprises inhibiting disturbing elements except those of a type that affects an input to the logic block from at least one of the flip-flops.

23. A scan test method as defined in claim 16, wherein inhibiting all of the disturbing elements except disturbing elements of a selected type comprises inhibiting disturbing elements except those of a type that affects an output of the logic block to at least one of the flip-flops.

24. A scan test method as defined in claim 16, wherein performing a scan test of disturbing elements of a selected type comprises inhibiting the selected disturbing elements to load a test vector into the flip-flops and enabling the selected disturbing element to observe operation of the logic block in response to the test vector.

25. A scan test method as defined in claim 16, wherein performing a scan test of the selected disturbing elements comprises scan testing the selected disturbing elements in active and inactive states.

26. A scan test method as defined in claim 16, wherein performing a scan test of the selected disturbing element comprises:

loading into the flip-flops, with all disturbing elements inhibited, a first test vector for scan testing a first disturbing element in an active state;

enabling the first disturbing element with all other disturbing elements inhibited;

observing operation of the logic block in response to the first test vector;

loading into the flip-flops, with all disturbing elements inhibited, a second test vector for scan testing the first disturbing element in an inactive state;

enabling the first disturbing element with all other disturbing elements inhibited; and

observing operation of the logic block in response to the second test vector.



INTEGRATED CIRCUIT TESTING METHOD AND SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an improved method and system for functionally testing an integrated circuit.

2. Discussion of the Related Art

5 In a functional testing, it is checked whether an integrated circuit performs the functions for which it has been designed. Predetermined signals are provided to the inputs of the circuit or of determined circuit blocks and the outputs are read to determine whether they correspond to an expected answer. To test all the possible errors of an integrated circuit, a first approach consists of providing the integrated circuit with all the possible combinations of input states and of checking all
10 the signals provided as a response by the circuit. This, however, can take a long time. Error models enable determining the test signals (or test vectors) most adapted to testing a circuit.

A so-called scan test method, applied to a logic block of an integrated circuit, having each of its inputs connected to an output terminal of a flip-flop and each of its outputs connected to an input terminal of a flip-flop, will more specifically be considered herein. A scan test system includes means
15 for controlling the writing and the reading of test signals in said flip-flops.

Fig. 1 schematically shows a scan test system associated with an integrated circuit including a combinatorial logic block, or logic block LB. The circuit includes three flip-flops FF1, FF2, and FF3. Input and output terminals D1 and Q1 of flip-flop FF1 are respectively coupled to an output terminal O1 and to an input terminal I1 of block LB. Similarly, the input and output terminals D2, Q2, and D3, Q3 of flip-flops FF2 and FF3 are respectively coupled to output and input terminals O2, I2, and O3, I3 of block LB. Clock terminals CK1, CK2, and CK3 of flip-flops FF1, FF2, and FF3 receive a same clock signal CLK. Flip-flops FF1, FF2, and FF3, as well as logic block LB, form the functional part of the circuit. The circuit test system includes multiplexers Mi (where i ranges between 1 and 3), each associated with the flip-flop FFi of same rank. The output terminal of each multiplexer Mi is connected to the input Di of same rank. A first input terminal of each multiplexer Mi is connected to output terminal Oi of block LB. A control terminal of each multiplexer Mi receives a signal SC. The second input terminal of multiplexer M1 is connected to an input terminal SI of the circuit. The second input terminals of multiplexers M2 and M3 are respectively connected to output
25

terminals Q1 and Q2 of flip-flops FF1 and FF2. Terminal Q3 of flip-flop FF3 is connected to an output terminal SO of the circuit.

Outside of test periods, signal SC is inactive and multiplexers Mi are controlled so that outputs Oi of the logic block are connected to inputs Di of flip-flops FFi. When signal SC is active, multiplexers Mi are controlled so that flip-flops FFi form a FIFO-type test register rated by clock signal CLK.

Fig. 2 schematically illustrates the operation of the test system of Fig. 1.

In a first step, signal SC is maintained active so that flip-flops FF1, FF2, and FF3 form the test register. Test data TD3, TD2, and TD1 are successively presented to terminal SI at the rate of pulses of clock signal CLK, at times t1, t2, and t3. At time t3, data TD3, TD2, and TD1 are respectively stored in flip-flops FF3, FF2, and FF1. Data TD3', TD2', and TD1' are then presented on output terminals O3, O2, and O1 of logic block LB.

In a second step, after time t3, signal SC is made inactive so that the multiplexers connect output terminals O3, O2, and O1 of the logic block to input terminals D3, D2, and D1 of the flip-flops. At the next pulse of signal CLK, at a time t4, data TD3', TD2', and TD1' are stored in flip-flops D3, D2, and D1. Signal SC is made active again after time t4.

In a third step, starting from the reactivation of signal SC, data TD3', TD2', and TD1' are shifted in the test register at the rate of pulses of clock signal CLK, at times t5 and t6, and are successively provided to terminal SO. During this shift, a new test vector TD6, TD5, TD4 is input in the register. Data TD3', TD2', and TD1' provided to terminal SO are compared with their expected values, generally logic "0s" or "1s".

These three steps are repeated as many times as test vectors have been provided. The analysis of the data provided by the logic block as a response to the test data, collected during each third step, enables determining whether the circuit includes defective elements. A defective element is, according to the error model conventionally used, an element having an output abnormally fixed to 0 or to 1. Such a test system operates satisfactorily if the logic block includes no element capable of disturbing the operation of the test register, or to disturb the propagation of the signals in the logic block. Even if such disturbing elements exist, existing test systems are adapted to inhibiting them.

Fig. 3 schematically shows a test system for an integrated circuit similar to the circuit shown in Fig. 1, in which three types of disturbing elements have been inserted.

A first disturbing element is an AND gate 2, a first input of which receives clock signal CLK, the second input of which is coupled to a clock enable signal EN1 generated in block LB, and the output of which is connected to terminal CK2. Gate 2 is capable of disturbing the sequencing of the test register, if for example data provided to block LB cause the inactivation of signal EN1 and the blocking of flip-flop FF2. The flip-flop assembly can then no longer operate as a shift register during the test. To solve this type of problem and make the circuit testable, a solution provided in prior art consists of adding an OR gate 4, the output terminal of which is connected to the second input terminal of AND gate 2, a first input terminal of which receives clock enable signal EN1, and a second input terminal of which receives a control signal TEST. When the circuit is not tested, signal TEST is made inactive, gate 4 transmits signal EN1 to gate 2 without influencing the circuit operation. When the circuit is tested, signal TEST is activated, the output of gate 4 remains activated whatever signal EN1, and gate 2 is no longer capable of disturbing the sequencing of the test register.

A second disturbing element is an element 5 which provides a reset signal RS to a reset terminal RST of flip-flop FF3 via an output terminal O5. Element 5 is capable of disturbing the sequencing of the test register, if for example test data provided to block LB cause the activation of signal RS and the resetting of flip-flop FF3. To make the circuit testable, a multiplexer 6 having an output terminal connected to terminal RST of flip-flop FF3 and a first input terminal connected to output O5 of the logic block has been added. A second input of multiplexer 6 receives a controllable signal TRST, for example permanently inactive. When the circuit is not tested, signal TEST is made inactive and multiplexer 6 transmits signal RS without influencing the circuit operation. When the circuit is tested, signal TEST is made active and multiplexer 6 permanently provides controllable signal TRST to terminal RST of flip-flop FF3. Thereby, block 5 is not capable of disturbing the sequencing of the test register.

A third disturbing element is a switch 8 capable of disturbing the propagation of a signal OD provided by block LB to output terminal O1. Terminal O1 is connected to a signal storage element 9 and switch 8 receives a signal EN2 generated by block LB. Switch 8 is capable of disturbing the circuit testing, especially during a second step of the testing, if test data provided to block LB cause the inactivation of signal EN2 and the opening of switch 8. Storage element 9 then provides the last value of the signal that it has received. The logic circuit is no longer combinatorial and it is no longer testable by scanning. To make the circuit testable, an OR gate 10, an output of which is connected to

According to an embodiment of the present invention, elements of a first type condition the clock signal provided to at least one flip-flop.

According to an embodiment of the present invention, elements of a second type condition a reset signal provided to at least one flip-flop.

5 According to an embodiment of the present invention, elements of a third type include locking elements capable of preventing the propagation of at least one signal into the logic block.

The present invention also aims at a method for testing an integrated circuit including flip-flops connected to a logic block, especially including the steps of:

a) connecting the flip-flops as a register and inhibiting the elements of the logic block capable
10 of disturbing the register sequencing, these elements being gathered in sets of elements of same type, then writing a test vector into the register,

b) reactivating a set of elements, then clocking the flip-flops, and

c) inhibiting again the set of reactivated elements before sequentially reading the data
contained in the register.

15 According to an embodiment of the present invention, step b) also includes deactivating the register connection of the flip-flops before clocking the flip-flops, and step c) also includes reactivating the register connection of the flip-flops before sequentially reading the data contained in the register.

20 The foregoing objects, features and advantages of the present invention, will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1, previously described, schematically shows a conventional system for testing by scanning an integrated circuit;

Fig. 2, previously described, illustrates the operation of the test system of Fig. 1;

25 Fig. 3, previously described, schematically shows a conventional integrated circuit scan test system including elements disturbing the test system;

Fig. 4 schematically shows an embodiment of a test system according to the present invention;

Fig. 5 illustrates the testing of a first disturbing element of the circuit of Fig. 4;

Fig. 6 illustrates the testing of a second disturbing element of the circuit of Fig. 4;

Fig. 7 illustrates the testing of a third disturbing element of the circuit of Fig. 4; and

Fig. 8 schematically shows an embodiment of a test system according to the present
5 invention.

DETAILED DESCRIPTION

Fig. 4 schematically shows a scan test system according to the present invention, associated with an integrated circuit such as shown in Fig. 3. The test system includes multiplexers Mi and inhibiting means 4, 6, and 10, identical to the elements bearing the same references in Fig. 3, connected in a similar way except for their control terminals. According to the present invention, each
10 type of inhibiting means is controlled by a specific control signal. Inhibiting means 4, 6 and 10 respectively receive a control signal TEST1, TEST2, and TEST3 provided by a control means 12. Also according to the present invention, multiplexers Mi are controlled by a control signal SC1 provided by control means 12, which receives control signal SC. Control means 12 is provided to generate signals TEST1, TEST2, TEST3, and SC1 based on signal SC.

15 When idle, the test system according to the present invention has no influence upon the circuit operation.

According to a first operating mode, a control means 12 provides multiplexers Mi with a signal SC1 identical to signal SC and it maintains control signals TEST1, TEST2, and TEST3 active. Thus, inhibiting means 4, 6, and 10 are activated and the effect of the disturbing elements is inhibited.
20 The operation of the test system is then similar to the operation of the test system of Fig. 3. This first operating mode enables performing a conventional scan test of the circuit. During this first operating mode, disturbing elements 2, 5, and 8 are not tested.

According to a second operating mode, illustrated by Figs. 5, 6, and 7, control means 12 successively controls the testing of each disturbing element, especially by temporarily inhibiting the
25 effects of the tested disturbing element, and by permanently inhibiting the effects of the other untested disturbing elements. For reasons of writing simplicity, references TD1 to TD6 and t1 to t6 already used in Fig. 2, but which represent different test data and times in the different drawings, are used in the following Figs. 5, 6, and 7.

Fig. 5 illustrates the testing of disturbing element 2. During the entire testing duration, control signals TEST2, TEST3, and SC1 are maintained active, so that flip-flops FF1, FF2, and FF3 form the test register and that the effect of disturbing elements 5 and 8 is inhibited. Control signal TEST1 is equal to signal SC received by block 12.

5 In a first step, signal TEST1 is maintained active so that signal EN1 provided by block LB to element 2 is not capable of disturbing the sequencing of the test register. Test data TD3, TD2, and TD1 are successively presented to terminal SI at the rate of the pulses of clock signal CLK, at times t1, t2, and t3, so that data TD3, TD2, and TD1 are respectively stored in flip-flops FF3, FF2, and FF1 from time t3. The test vector corresponding to data TD3, TD2, and TD1 is chosen to give to logic
10 block LB a state such that signal EN1 is normally active.

In a second step, a predetermined duration after time t3, signal TEST1 is made inactive so that gate 4 transmits signal EN1 to element 2. If element 2 or its connection exhibits an error and signal EN1 is inactive, instead of being active as it should be, flip-flop FF2 is not clocked at the next pulse of signal CLK, at a time t4. Datum TD2 then remains stored in flip-flop FF2 after time t4, while
15 datum TD1 should have been input into flip-flop FF2.

In a third step, control signal TEST1 is made active again, a predetermined duration after time t4. The data contained in flip-flops FF1, FF2, and FF3 are shifted in the test register at the rate of the pulses of clock signal CLK, at times t5 and t6, and successively provided to terminal SO to be analyzed.

20 At times t4, t5, and t6, a new test vector TD6, TD5, and TD4 is input into the test register. This new test vector is chosen to give the logic block a state in which signal EN1 is normally inactive. The preceding second and third steps are then repeated to check that element 2 or its connection do not include an error that maintains signal EN1 active.

Fig. 6 illustrates the testing of disturbing element 5. Control signals TEST1, TEST3, and SC1
25 are maintained active, so that flip-flops FF1, FF2, and FF3 form the test register and the effect of disturbing elements 2 and 8 is inhibited. Control signal TEST2 is equal to signal SC received by block 12.

In a first step, signal TEST2 is maintained active so that signal RS provided by element 5 is not capable of disturbing the sequencing of the test register. Test data TD3, TD2, and TD1 are
30 successively presented to terminal SI at the rate of pulses of clock signal CLK, at times t1, t2, and t3,

so that data TD3, TD2, and TD1 are respectively stored in flip-flops FF3, FF2, and FF1 and provided to input terminals I3, I2, and I1 from time t3. Data TD3, TD2, and TD1 form a test vector intended for controlling the activation of signal RS by element 5. Thus, in a normal operation of the logic block, signal RS would cause a reset of the content of flip-flop FF3. During the first step, nothing
5 occurs due to the presence of signal TEST2 in an active state.

In a second step, at a time t3' subsequent to time t3, control signal TEST2 is made inactive so that signal RS directly controls the reset terminal of flip-flop FF3. If element 5 or its connection includes an error that maintains signal RS inactive, flip-flop FF3 is not reset and datum TD3 remains stored in flip-flop FF3 during the period shown with hatchings in Fig. 6. Further, at the next pulse of
10 signal CLK, which occurs at a time t4, datum TD2 is stored in flip-flop FF3 instead for flip-flop FF3 to remain reset. If signal RS is active, datum TD3 is replaced in flip-flop FF3 by a reset value and flip-flop FF3 remains reset after time t4.

In a third step, control signal TEST2 is made active again, a predetermined duration after time t4. At time t4 and at times t5 and t6 representing the next pulses of clock signal CLK, a new test
15 vector TD6, TD5, and TD4 is input into the test register. Vector TD6, TD5, and TD4 is chosen to give the logic block a state in which signal RS is deactivated by element 5. The preceding second step is then repeated to check that element 5 or its connection does not include an error that maintains signal RS active.

Fig. 7 illustrates the testing of disturbing element 8. Control signals TEST1 and TEST2 are
20 maintained active so that the effect of disturbing elements 2 and 8 is not inhibited. Control signals TEST3 and SC1 are equal to signal SC received by block 12.

In a first step, control signal SC1 is made active so that flip-flops FF1, FF2, and FF3 form the test register. Control signal TEST3 is also active, and the propagation of signal OD provided by block LB to terminal O1 is not capable of being disturbed by switch 8, whatever the value of signal EN2
25 provided to switch 8. Test data TD3, TD2, and TD1 are successively presented to terminal SI at the rate of pulses of clock signal CLK, at times t1, t2, and t3, so that data TD3, TD2, and TD1 are respectively stored in flip-flops FF3, FF2, and FF1 and provided to input terminals I3, I2, and I1 from time t3. The data which are then presented on outputs O3, O2, and O1 of block LB are called TD3', TD2', and TD1'. Storage element 9 stores value TD1'.

The control means, of simple structure, has a reduced size. Thus, a test system according to the present invention has substantially the same size as a conventional scan test system, which is an additional advantage of the present invention.

Further, since the present invention provides isolating the testing of each type of disturbing
5 element, the test vectors used for each type of disturbing element can be generated automatically and rapidly by a calculator having a list of the circuit elements and of their connections. This is an additional advantage of the present invention.

Of course, the present invention is likely to have various alterations, modifications, and improvements which will readily occur to those skilled in the art. Disturbing elements 2, 5, and 8
10 shown in Fig. 4 are shown as an example only. There are many types of elements disturbing the scan test, generally known as "exceptions to the rules of scan testability", and those skilled in the art will easily adapt the present invention to the types of disturbing elements which have not been shown herein.

Fig. 8 schematically shows an embodiment of a test system according to the present
15 invention, adapted to the testing of a specific disturbing element 8. The preceding disturbing elements 2 and 5 have not been shown in Fig. 8. In Fig. 8, signal OD is directly provided by the output of flip-flop FF2, and terminal O1 and storage element 9 are connected to a three-state bus TB. Bus TB further receives signals OD4, OD5, OD6 via switches 18, 20, and 22. Switches 18, 20, and 22 receive signals EN4, EN5, EN6 from block LB. Switch 8 is controlled by a NOR gate receiving signals EN4,
20 EN5, EN6 and the inverse of signal TEST3 as an input. When signal TEST3 is activated, terminal O1 is controlled either by signals OD4, OD5, OD6, or by flip-flop FF2, and the circuit remains combinatorial whatever the state of signals EN4, EN5, EN6.

The test steps and vectors of disturbing elements 2, 5, and 8 have also been described as an example, but those skilled in the art will easily adapt the present invention to other test steps and to
25 other test vectors.

The present invention has been described in relation with a circuit including a single logic block and three flip-flops, but those skilled in the art will easily adapt the present invention to a circuit including a greater number of logic blocks and/or a greater number of flip-flops. If the circuit includes several logic blocks, each logic block may be tested separately.

(Page 1 of 2)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,938,194 *B2*
DATED : August 30, 2005
INVENTOR(S) : Jacques Prunier

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 1, lines 46-47 should read:

--each multiplexer Mi is connected to the input Di of same rank. A first input terminal of each multiplexer Mi is connected to --

Col. 1, line 66 should read:

--TD3, TD2, and TD1 are successively presented to terminal SI at the--

Col. 3, line 1 should read:

--circuit operation. When the circuit is tested, signal TEST is --

Col. 4, line 22 should read:

--before sequentially reading the data contained in the register.--

Col. 4, line 55 should read:

--elements bearing the same references in Fig. 3, connected in --

Col. 5, line 55 should read:

--do not include an error that maintains signal EN1 active.--

Col. 6, line 23 should read:

--test register. Vector TD6, TD5, and TD4 is chosen to give the--

Col. 6, line 42 should read:

--and FF1 and provided to input terminals I3, I2, and I1 from time t3--

Col. 7, line 42 should read:

--readily occur to those skilled in the art. Disturbing elements--

MAILING ADDRESS OF SENDER

PATENT NO. 6,938,194

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SEP 15 2005

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,938,194 *B2*
DATED : August 30, 2005
INVENTOR(S) : Jacques Prunier

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 7, line 44 should read:

-- There are many types of elements disturbing the scan test,--

Col. 8, line 2 should read:

--a single logic block and three flip-flops, but--

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